Claims

1. A feed forward clock and data recovery unit for recovering a received serial data bit stream having:

(a) feed forward phase tracking means for tracking of a sampling time to the center of a unit interval (UI) of the received data bit stream, wherein the feed forward phase tracking means comprises:

(a1) sampling phase generation means for generating equidistant sample phase signals which are output with a predetermined granularity;

(a2) an oversampling unit (OSU) for oversampling the received data bit stream with the sample phase signals according to a predetermined oversampling rate (OSR);

(a3) a serial-to-parallel-conversion unit which converts the oversampled data stream into a deserialized data stream with a predetermined decimation factor (DF);

(a4) a binary phase detection unit (BPD) for detecting an average phase difference (AVG-PH) between the received serial data bit stream and the sample phase signal by adjusting a phase detector gain (PDG) depending on the actual data density (DD) of the deserialized data stream such that the variation of the average phase detection gain (PDG) is minimized; and

(a5) a loop filter for tracking of small phase offset of the detected average phase signal (AVG-PH) around an ideal sampling time at the center of the unit interval (UI) to generate a fine track control signal;

(a6) a finite state machine (FSM) which detects whether the average phase signal has exceeded at least one

predetermined phase threshold value and which generates a corresponding coarse shift control signal;

(a7) a binary rotator which rotates the deserialized data bit stream in response to the coarse shift control signal and in response to the fine track control signal;

(b) data recognition means (DRM) for recovery of the received data stream which includes a number of parallel data recognition FIR-Filters, wherein each data recognition FIR-Filter comprises:

(b1) a weighting unit for weighting data samples of the deserialized data stream which has been adjusted to the ideal sampling time by the binary rotator;

(b2) a summing unit for summing up the weighted data samples; and

(b3) a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

2. The feed forward clock and data recovery unit according to claim 1 wherein a bit alignment unit is provided which applies data samples generated by the oversampling unit within one unit interval (UI) simultaneously to the serial-to-parallel-conversion unit.

3. The feed forward clock and data recovery unit according to claim 1 wherein the finite state machine comprises a first memory for storing at least one phase threshold value; and

a second memory for storing for each phase threshold value the corresponding coarse shift coefficient (A_i).

4. The feed forward clock and data recovery unit according to claim 3 wherein the finite state machine comprises a comparator for comparing the average phase difference with the at least one phase threshold value and outputs a corresponding coarse shift coefficient.

5. The feed forward clock and data recovery unit according to claim 3 wherein the phase threshold values are programmable.

6. The feed forward clock and data recovery unit according to claim 3 wherein the coarse shift coefficients are programmable.

7. The feed forward clock and data recovery unit according to claim 3 wherein the finite state machine comprises a multiplicator for multiplying a coarse shift coefficient output by said comparator with a sign value of the average phase difference (AVG-PH).

8. The feed forward clock and data recovery unit according to claim 1 wherein the binary rotator comprises a shift register for storing data samples of the deserialized data stream over more than one unit interval (UI), and a barrel shifter which rotates all data samples of one unit interval (UI) and some neighboring data samples of a preceeding and of a following unit interval in response to the coarse shift control signal and in response to the fine track control signal.

9. The clock and data recovery unit according to claim 1 wherein the binary phase detection unit (BPD) comprises:

means for detecting the actual data density (DD) of the deserialized data bit stream; and

means for adjusting the phase detector gain (PDG) depending on the detected actual data density (DD).

10. The clock and data recovery unit according to claim 9 wherein the means for detecting the actual data density comprises a plurality of EXOR gates,

wherein each EXOR gate compares two neighboring data samples generated by the oversampling unit to decide whether a data transition has occurred.

11. The clock and data recovery unit according to claim 10 wherein the means for detecting the actual data density further comprises summation means for accumulating the number of transitions detected by the EXOR gates.

12. The clock and data recovery unit according to claim 9 wherein the means for adjusting the phase detector gain calculates the phase detector gain (PDG) by multiplying the accumulated number of transitions with a multiplication factor (MF).

13. The clock and data recovery unit according to claim 12 wherein the multiplication factor (MF) is increased when the detected number of transitions is decreased.

14. The clock and data recovery unit according to claim 10 wherein the number (N) of EXOR gates for detection of the actual data density is given by the product of the decimation factor (DF) of the serial-to-parallel-conversion unit and the oversampling rate (OSR) of the oversampling unit ($N = DF \times OSR$).

15. The clock and data recovery unit according to claim 1 wherein the decimation factor (DF) of the serial to parallel conversion unit is eight ($DF = 8$).

16. The clock and data recovery unit according to claim 1 wherein the oversampling rate (OSR) of the oversampling unit is four (OSR = 4).

17. The clock and data recovery unit according to claim 1 wherein the data transmission rate (DR) of the serial data bit stream is more than one Gigabit per second (DR ≥ 1 Gbit/sec).

18. The clock and data recovery unit according to claim 1 wherein the weighting unit of the data recognition means comprises signal amplifiers, wherein each signal amplifier amplifies a respective data sample with a programmable gain.

19. The clock and data recovery unit according to claim 1 wherein the data recognition FIR-Filters of the data recognition means are connected to a FIFO-memory.

20. The clock and data recovery unit according to claim 1 wherein the number of data recognition FIR-Filters corresponds to the decimation factor (DF) of the serial-to-parallel-conversion unit.

21. The clock and data recovery unit according to claim 1 wherein the oversampling unit (OSU) comprises a predetermined number of clock triggered sampling elements.

22. The clock and data recovery unit according to claim 21 wherein the sampling elements are D-Flip-Flops.

23. The clock and data recovery unit according to claim 21 wherein the sampling elements are D-Latches.

24. The clock and data recovery unit according to claim 21 wherein each sampling element is clocked by a corresponding sampling phase signal generated by the sampling phase generator means.

25. The clock and data recovery unit according to claim 1 wherein the sampling phase generating means receives a reference clock signal from a reference clock generator.

26. The clock and data recovery unit according to claim 25 wherein the reference clock generator is a phase locked loop (PLL).

27. The clock and data recovery unit according to claim 1 wherein the sampling phase generating means comprises a delay locked loop (DLL) for generating equidistant phase signals.

28. The clock and data recovery unit according to claim 27 wherein the sampling phase generating means further comprises a phase interpolation unit.

29. The clock and data recovery unit according to claim 27 wherein the equidistant phase signals have a phase difference $\Delta\varphi$ of 45° to define eight phase segments.

30. The clock and data recovery unit according to claim 28 wherein the phase interpolation unit interpolates sample phase signals on the basis of the equidistant phase signals generated by the delay locked loop (DLL).

31. The clock and data recovery unit according to claim 1 wherein a lock detection unit is provided which detects whether the clock and data recovery unit is locked to the received serial data bit stream.

32. The clock and data recovery unit according to claim 1 wherein a transition loss the detection unit is provided which detects when the serial data bit stream has stopped.

33. The clock and data recovery unit according to claim 1 wherein the feed forward phase tracking means and the data recognition means are integrated in a digital control unit.

34. The clock and data recovery unit according to claim 27 wherein the digital control unit further includes the lock detection unit and the transition loss detection unit.

35. A feed forward clock and data recovery unit for recovering a received serial data bit stream having:

(a) feed forward phase tracking means for tracking of a sampling time to the center of a unit interval (UI) of the received data bit stream, wherein the feed forward phase tracking means comprises:

(a1) sampling phase generation means for generating equidistant sample phase signals which are output with a predetermined granularity;

(a2) an oversampling unit (OSU) for oversampling the received data bit stream with the sample phase signals according to a predetermined oversampling rate (OSR);

(a3) a binary phase detection unit (BPD) for detecting an average phase difference (AVG-PH) between the received serial data bit stream and the sample phase signal by adjusting a phase detector gain (PDG) depending on the actual data density (DD) of the data stream such that the variation of the average phase detection gain (PDG) is minimized; and

(a4) a loop filter for tracking of small phase offset of the detected average phase signal (AVG-PH) around an ideal sampling time at the center of the unit interval (UI) to generate a fine track control signal;

(a5) a finite state machine (FSM) which detects whether the average phase signal has exceeded at least one predetermined phase threshold value and which generates a corresponding coarse shift control signal;

(a6) a binary rotator which rotates the deserialized data bit stream in response to the coarse shift control signal and in response to the fine track control signal;

(b) a data recognition unit (DRM) for recovery of the received data stream which includes a number of parallel data recognition filters, wherein each data recognition filter comprises:

(b1) a weighting unit for weighting data samples of the data stream which has been adjusted to the ideal sampling time by the binary rotator;

(b2) a summing unit for summing up the weighted data samples; and

(b3) a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

36. Method for clock and data recovery of a received serial data bit stream comprising the following steps:

(a1) oversampling the received data bit stream with sampling phase signals having a predetermined granularity;

(a2) detecting an average phase difference (AVG-PH) between the received serial data bit stream and sampling phase signals by adjusting a phase detector gain (PDG) depending on the data density (DD) of the data stream to

minimize the variation of the average phase detector gain;

(a3) filtering the detected average phase difference to generate a fine track control signal provided for tracking a small phase of the average phase signal around an ideal sampling time of the center of the unit interval (UI);

(a4) comparing the detected average phase difference with at least one threshold value to generate a coarse shift control signal;

(a5) rotating the data stream in response to the coarse shift control signals and in response to the fine track control signal by means of a binary rotator;

(b1) weighting data samples of the data stream around the ideal sampling time;

(b2) summing up the weighted data samples;

(b3) comparing the summed up weighted data samples with a threshold value to detect the logic value of the data bit within the serial data bit stream.

Reference list

1	feed forward clock and data recovery unit
2	data input
3	data output
4	reference clock input
5	clock output
6	loss indicating output
7	lock indicating output
8	delay locked loop
9	phase interpolation unit
10	oversampling unit
11	bit alignment unit
12	serial-to-parallel-conversion unit
13	digital control unit
14	register
15	register
16	register
17	internal clock line
18	binary phase detector
19	buffer
20	tracking loop filter
21	finite state machine
22	binary rotator
23	data recognition unit
24	FIFO
25	Transition loss detection unit
26	lock detection unit